

Serial No. 10/708,340
Hiroyuki Akatsu et al.

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In the Claims:

1-7. (cancelled)

8. (currently amended) A bipolar transistor, comprising:

a collector including a frustum-shaped collector pedestal having an at least substantially planar upper surface extending in lateral directions, a lower surface, and a slanted sidewall extending between said upper surface and said lower surface, wherein said upper surface has an area substantially less than an area of said lower surface;

an intrinsic base overlying all of said area of said upper surface of said collector pedestal;

an emitter overlying said intrinsic base;

an extrinsic base conductively connected to said intrinsic base; and

a first dielectric region laterally adjacent to said emitter; and

a second dielectric region laterally adjacent to said collector pedestal.

wherein an opening extending extends through said first and second dielectric regions, said opening defining edges of having a wall extending through said first and second dielectric regions, said edges being aligned in a vertical direction transverse to said lateral directions, said emitter having an edge referenced to said ~~wall of said opening~~ edge of said first dielectric region and said collector pedestal having an edge referenced to said edge of said second dielectric region wall, such that said emitter is aligned with said collector pedestal.

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9. (cancelled)

10. (previously presented) A bipolar transistor as claimed in claim 8, wherein said intrinsic base includes a layer of a single-crystal semiconductor which forms a heterojunction with at least one of said emitter and said collector pedestal.

11-20. (cancelled)

21. (currently amended) bipolar transistor as claimed in claim 8, further comprising a ~~dielectric filled shallow trench isolation and a~~ conductive collector contact via, said collector further including a single-crystal semiconductor region having a first active area underlying said lower surface of said collector pedestal and first active area and a second active area separated in at least one of said lateral directions from said first active area by a shallow trench isolation extending to a depth below said lower surface of said collector pedestal disposed in a single-crystal semiconductor region, each of said first and second active areas having major surfaces extending in lateral directions defining a major surface of said semiconductor region, said first active area underlying said collector pedestal and said second active area being separated in at least one of said lateral directions from said first active area by said shallow trench isolation, wherein said collector contact via overlies said second active area.

22. (currently amended) A bipolar transistor as claimed in claim 8, wherein at least a portion of said extrinsic base is raised above an upper surface of said intrinsic base, wherein a wall an edge of said raised portion of said extrinsic base is aligned in the vertical direction with said edges of wall of said opening in said first and second dielectric regions.

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23. (previously presented) A bipolar transistor as claimed in claim 22, further comprising a solid dielectric spacer spacing said raised portion of said extrinsic base from said emitter, said solid dielectric spacer including (a) a first dielectric spacer wholly contacting a wall of said raised portion of said extrinsic base, and (b) a second dielectric spacer contacting an inner wall of said first dielectric spacer remote from said raised portion of said extrinsic base.

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